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JP11120092A2: METHOD AND DEVICE FOR HIGH AVAILABILITY AND CACHING PROCESS OF DATA STORAGE DEVICE

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Country:	**JP** Japan
Kind:	
Inventor(s):	**CHONG FAY**
Applicant(s):	**SUN MICROSYST INC** News, Profiles, Stocks and More about this company
Issued/Filed Dates:	**April 30, 1999** / June 26, 1998
Application Number:	**JP1998000181019**
IPC Class:	**G06F 13/00**; G06F 3/06;
Priority Number(s):	June 26, 1997 **US1997000883923**

Abstract:
Problem to be solved: To provide the high availability and efficient caching process of the data storage device.
Solution: A fiber channel circuit as this device consists of a main controller 16, a subcontroller 22 which has the same address with the main controller 16, a switching circuit 12 which is coupled with the main controller 16 and subcontroller 22, and a control circuit 14 which is coupled with the switching circuit 12. In normal operation, the control circuit 14 sets the switching circuit 12 so that the main controller 16 receives and responds to input data supplied from a host and the subcontroller 22 receives the input data. In fail-over operation wherein the main controller gets out of order, the main controller is disabled and the control circuit sets the switching circuit so that the subcontroller receives the input data supplied from the host and responds to it. The fail-over is transparent to the host.
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Other Abstract Info: DERABS G1999-062879

Foreign References: (No patents reference this one)

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(AB) U.S. Class   (123) U.S. Class   **TDB** IBM Technical

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PATENT ABSTRACTS OF JAPAN

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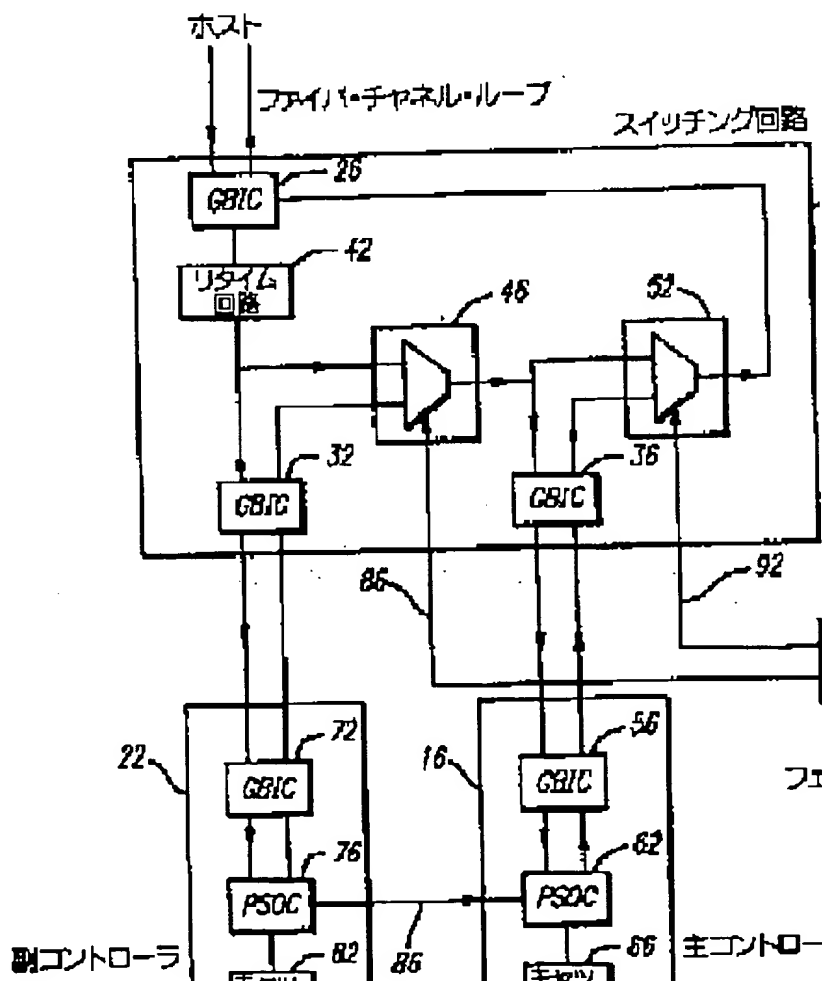| (30) Priority:	26.06.97 US 97 883923	
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(54) **METHOD AND DEVICE FOR HIGH AVAILABILITY AND CACHING PROCESS OF DATA STORAGE DEVICE**

(57) Abstract:

PROBLEM TO BE SOLVED: To provide the high availability and efficient caching process of the data storage device.

SOLUTION: A fiber channel circuit as this device consists of a main controller 16, a subcontroller 22 which has the same address with the main controller 16, a switching circuit 12 which is coupled with the main controller 16 and subcontroller 22, and a control circuit 14 which is coupled with the switching circuit 12. In normal operation, the control circuit 14 sets the switching circuit 12 so that the main controller 16 receives and responds to input data supplied from a host and

supplied from a host and the subcontroller 22 receives the input data. In fail-over operation wherein the main controller gets out of order, the main controller is disabled and the control circuit sets the switching circuit so that the subcontroller receives the input data supplied from the host and responds to it. The fail-over is transparent to the host.

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ホスト

ファイバ・チャネル・ループ

スイッチング回路

12

GBIC *26*

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22

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GBIC *56*

PSOC *76*

PSOC *62*

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